List of Claims:

1-4. (Canceled)

5. (Currently Amended) A selectable resolution image capture system comprising:

an imager having a plurality of photocells that produce an analog electrical response to light exposure;

a circuit that converts the electrical responses of the plurality of photocells into digital signals;

the circuit having a full-resolution mode and a low-resolution mode; ~~and~~

an image processor that operates the circuit and selects between the full-resolution and low-resolution modes of the circuit to capture an image, where the image processor detects whether there is a low incident light condition, and in response to detecting the low incident light condition, the image processor switches from the full-resolution mode to the low-resolution mode of the circuit and captures the image using the low-resolution mode of the circuit;

a row clock signal operating at a first clock rate;

a column clock signal operating at a second clock rate; and

a charge accumulator configured to accumulate charges from selected photocells during first clock cycles;

wherein the image processor increases the first clock rate and the second clock rate during second clock cycles when the charge accumulator is not accumulating charges.

6. (Currently Amended) A selectable resolution image capture system comprising:

an imager having a plurality of photocells that produce an analog electrical response to light exposure;

a circuit that converts the electrical responses of the plurality of photocells into digital signals;

the circuit having a full-resolution mode and a low-resolution mode; ~~and~~

an image processor that operates the circuit and selects between the full-resolution and low-resolution modes of the circuit to capture an image, where the image processor detects whether there is a low power condition, and in response to detecting the low power condition, the image processor switches from the full-resolution mode to the low-resolution mode of the circuit and captures the image using the low-resolution mode of the circuit;

a row clock signal operating at a first clock rate;

a column clock signal operating at a second clock rate; and

a charge accumulator configured to accumulate charges from selected photocells during first clock cycles;

wherein the image processor increases the first clock rate and the second clock rate during second clock cycles when the charge accumulator is not accumulating charges.

7-25. (Canceled)

26. (Currently Amended) A ~~The~~ selectable resolution image capture system ~~of claim 5~~ comprising:

an imager having a plurality of photocells that produce an analog electrical response to light exposure;

a circuit that converts the electrical responses of the plurality of photocells into digital signals, the circuit having a full-resolution mode and a low-resolution mode;

an image processor that operates the circuit and selects between the full-resolution and low-resolution modes of the circuit to capture an image;

a row clock signal operating at a first clock rate;

a column clock signal operating at a second clock rate; and

a charge accumulator configured to accumulate charges from ~~the~~ selected ~~pixels~~ photocells during first clock cycles;

wherein the image processor increases the first clock rate and the second clock rate during second clock cycles when the charge accumulator is not accumulating charges.

27-28. (Canceled)

29. (Currently Amended) A method of selecting a resolution of an image by an image capture system, the method comprising:

producing an analog electrical response to light exposure using a plurality of photocells;

converting the electrical responses of the plurality of photocells into digital signals using a circuit having a full-resolution mode and a low-resolution mode;

detecting whether there is a low incident light condition for the image;

switching from a full-resolution mode to a low-resolution mode in response to detecting the low incident light condition; ~~and~~

capturing the image using the low-resolution mode of the circuit;

providing a row clock signal operating at a first clock rate;

providing a column clock signal operating at a second clock rate;

accumulating charges from selected photocells using a charge accumulator during first clock cycles; and

increasing the first clock rate and the second clock rate during second cycles, when the charge accumulator is not accumulating charges.

30. (Canceled)

31. (Currently Amended) A method of selecting a resolution of an image by an image capture system, the method ~~The method of claim 29~~ comprising:

producing an analog electrical response to light exposure using a plurality of photocells;

converting the electrical responses of the plurality of photocells into digital signals using a circuit having a full-resolution mode and a low-resolution mode;

providing a row clock signal operating at a first clock rate;

providing a column clock signal operating at a second clock rate;

accumulating charges from ~~the~~ selected ~~pixels~~ photocells using a charge accumulator during first clock cycles; and

increasing the first clock rate and the second clock rate during second cycles, when the charge accumulator is not accumulating charges.